REMARKS

Claim Rejections Under 35 U.S.C. § 102

Claims 9, 13, 16-17, and 22 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Hara* (U.S. Patent No. 5,406,521). Claims 9, 13, 16-17 were also rejected under 35 U.S.C. § 102(e) as being anticipated by *Kawamura et al.* (U.S. Patent No. 5,406,524). Applicant respectfully traverses these rejections.

Claims 9, 13, and 22 have been amended to more clearly claim the subject matter that Applicant regards as the invention. Claims 9, 13, and 22 have been amended to include limitations making it clear that there are multiple sets of wordlines each coupled to a different row decoder. These claims have also been amended to make it clear that each isolation well is located in a different lower well. These limitations are disclosed in the specification at paragraph 0023 and drawings including Figure 4. Therefore, no new matter has been entered by this amendment.

Hara discloses a semiconductor memory device. Figure 1 shows a memory cell that is formed in a p-well 3 that is formed in an n-well 2 and both are formed on a p-substrate 1. Figure 2 shows a circuit of a memory cell array 10. Neither of these figures teach or suggest Applicant's invention as claimed in the amended claims.

The Examiner contends that Figure 1 shows a substrate of a second conductivity with a plurality of lower wells having a first conductivity with each lower well having an inner isolation well of the second conductivity. The Examiner further contends that Figure 2 shows a plurality of memory blocks, each memory block located in a different isolation well. However, these figures only show one isolation well within another well and a single memory cell or an entire memory array within that inner well. There is no teaching or suggestion in *Hara* that a plurality of memory blocks are each formed within different isolation wells as claimed in Applicant's amended claims. Further, there is no teaching or suggestion in *Hara* that each memory block is coupled to a first set of wordlines of a plurality of sets of wordlines as claimed by Applicant.

Kawamura et al. disclose a non-volatile semiconductor memory device. Figure 3 shows a memory cell in an inner p-well within an n-well on a p-type substrate. However, there is no teaching or suggestion that each memory block of a plurality of memory blocks is located within

a different isolation well as claimed in Applicant's amended claims. Further, there is no teaching or suggestion in *Kawamura et al.* that each memory block is coupled to a first set of wordlines of a plurality of sets of wordlines. *Kawamura et al.'s* teachings do not go beyond a single n-well with an inner p-well containing a memory cell.

Allowable Subject Matter

Claims 10-11 and 14-15 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims.

Claims 18-21 were allowed.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this amendment and response.

Respectfully submitted,

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